

CLAIMS

1. An oscillator circuit, comprising:

an oscillating unit comprising an inductance and
5 a variable capacitance element and generating a signal
having a frequency of n times a target frequency; and
a divider circuit dividing a signal generated by
the oscillating unit into $1/n$ frequency, wherein

10 the oscillating unit comprising an inductance and
a variable capacitance element, and the divider circuit
are formed on a semiconductor integrated circuit board.

2. An oscillator circuit, comprising:

an oscillating unit comprising an inductance and
15 a variable capacitance element and generating a signal
having a frequency of n times a target frequency;

a control voltage generation circuit generating
a control voltage for controlling an oscillation
frequency of the oscillating unit and outputting the
20 the control voltage to the oscillating unit; and

a divider circuit dividing a signal generated by
the oscillating unit into $1/n$ frequency, wherein

the oscillating unit comprising an inductance and
a variable capacitance element, the control voltage
25 generation circuit and the divider circuit are formed

on a semiconductor integrated circuit board.

3. The oscillator circuit either in claim 1 or 2,
wherein said oscillating unit comprises a plurality of
5 MOSFETs, an inductance and a variable capacitance
element.

4. The oscillator circuit in claim 2, wherein said
oscillating unit comprises a plurality of MOSFETs, an
10 inductance and a variable capacitance element, and said
control voltage generation circuit controls an
oscillation frequency of the oscillating unit by
outputting a control voltage to the variable capacitance
element for changing the capacitance of the variable
15 capacitance element.

5. The oscillator circuit either in claim 1, 2, 3 or
4 wherein said oscillating unit comprises a first and
a second MOSFETs, an inductance and a variable
20 capacitance element;

either the source or drain of the first MOSFET is
connected with the inductance and the variable
capacitance element; the gate of the first MOSFET is
connected with the source or drain of the second MOSFET;
25 and the gate of the second MOSFET is connected with the

source or drain of the first MOSFET.

6. The oscillator circuit in either one of claims 1 through 4, wherein said oscillating unit comprises a first and a second MOSFETs, an inductance, a capacitor and a variable capacitance element;

either the source or drain of the first MOSFET is connected with the inductance, the gate of the first MOSFET is connected with either the source or drain of the second MOSFET, the gate of the second MOSFET is connected with either the source or drain of the first MOSFET, and either the source or drain of the first MOSFET is connected with the variable capacitance element by way of the capacitor; and

a control voltage outputted from said control voltage generation circuit is applied to the variable capacitance element so as to change the capacitance thereof and thereby controlling an oscillation frequency.

20

7. The oscillator circuit in either one of claims 1 through 6, wherein said variable capacitance element comprises a MOSFET.

8. The oscillator circuit in either one of claims 2

through 7, wherein said control voltage generation circuit detects a phase difference between a divided signal of a signal generated by said oscillating unit and the reference signal, and outputs a control voltage
5 according to the phase difference.

9. The oscillator circuit in either one of claims 1 through 8, wherein said control voltage generation circuit is a PLL synthesizer circuit comprising a
10 programmable counter, a phase detection circuit comparing phases between a signal outputted from the programmable counter and the reference signal, and a low-pass filter blocking a high frequency component of an output signal of the phase detection circuit and
15 outputting a DC control voltage to said oscillating unit.

10. The oscillator circuit in either one of claims 1 through 9, wherein said divider circuit includes a divider circuit having a duty ratio of 50%.